REMARKS

Claims

Claims 1-17 remain pending in this application. No amendments to the claims have been made.

35 U.S.C. § 103

Claims 1-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamada, U.S. Patent No. 5,986,924 in view of Houston, U.S. Patent No. 6,611,451, Sim et al, U.S. Patent No. 6,456,555 and Ohbayashi et al, U.S. Patent No. 6,556,058. Applicants request reconsideration of the rejection for the following reasons.

According to the present invention, the leakage current of MOS transistors in SRAM memory cells can be reduced by controlling the electrical potential of a source line (ss1, Fig. 1) of memory cells. In particular, a source potential control circuit is provided, as set forth in claims 1 and 9. Further, in claim 17, the operational potential of the memory cells is claimed as being controlled. As set forth in claim 1, the source potential control circuit sets the supply potential to an intermediate potential between the ground potential and the supply potential. The source potential control circuit is also claimed as including an n-channel MOSFET connected between the source potential and the ground potential (e.g., claim 2) and further includes a resistance between the source line and the ground potential line (e.g., claim 3). The potential of ss1 is controlled such the leakage current is reduced by raising the potential of the source line ss1 while also ensuring that the data will not be damaged in a device having different transistor characteristics, such as Vth. See Figs. 5, 6A and 6B, for example, and the specification at page 13, lines 5-16 and page 15, lines 4-13, for example.

In Yamada, the SRAM disclosed in the prior art figure (Fig. 12) comprises a plurality of SRAM cells each having a driver MOSFET, transfer MOSFET, load MOSFET, switch transistor and resistor. In the Office Action it is alleged that although a diode-transistor is not shown, a diode could be used to connect the source line of the SRAM array to ground in view of the disclosure of Houston and the teachings of Sim, which show a diode-connected transistor in a memory device. Further, it is alleged that using a resistance element comprised of an channel-MOSFET having its gate connected to Vdd is suggested by Ohbayashi et al.

Applicants disagree that the references used in the rejection, when taken together, suggest the claimed combination of the invention set forth in claims 1-17. In Yamada, the nMOS transistor (36) is controlled to be off when the memory cell is not in operation, and the common source line Vss is connected to the ground line only through a high-resistance element (37). See col. 2, line 54 and Fig. 12 of the reference, for example. As such, Yamada discloses that a leakage current is reduced by raising the source potential of the memory cells to a level greater than Vss by use of a high-resistance element inserted between the source line and the ground line. However, Yamada does not disclose control of the source potential, as claimed by Applicants, that achieves a reduction in leakage current and ensures that the data will not be damaged, in a device having different transistor characteristics.

Houston discloses an approach to reducing the SRAM array leakage in a stand-by state by raising the array lower supply voltage (Vss array). This reduces the array leakage both by reducing the voltage across transistors in the array and by effectively applying a back-gate bias on the n-channel resistors, thereby raising their threshold

voltage. See Fig. 1 and column 1, line 22 of the reference, for example. Accordingly, Houston discloses that a leakage current is reduced by raising a source potential of the memory cells higher than the Vss level and the source potential is raised with a diode 24 inserted between the source line and the ground line. However, the reference does not support the modification to Yamada proposed in the Office Action since control of the source potential by a source potential control circuit equivalent to that of the present invention is not disclosed.

In Sim, various diode-connected MOS transistor configurations are disclosed that can be used as resistors, referring to col. 8, line 54 and figure 5 of the reference. However, a reduction of the leakage current of the memory cells is not discussed in the reference. In Ohbayashai, an n-channel MOS transistor is disclosed as constituting a resistance element as set forth in column 6, line 15, with respect to figure 1 of the reference. However, the reduction of a leakage current in memory cells is not disclosed in the reference. Therefore, the reference does not suggest the modification proposed in the Office Action in support of the 35 USC §103(a) rejection. Accordingly, the combination of Yamada in view of Yamada, Houston, Sim et al., and Ohbayashi et al. does not render claims 1-17 obvious under 35 USC §103(a), therefore the rejection should be withdrawn.